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Review on Performance Analysis of Content Addressable Memory Search Mechanisms

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Abstract

We surveyed recent techniques utilized in the construction of high-throughput low-energy Content available Memory (CAM).A CAM may be a memory that performs the lookup-table operation in a very single clock cycle using unique comparison electronic equipment.CAMs are particularly fashionable in network routers for packet forwarding and packet classification, however they're additionally useful in a variety of alternative applications that need high speed table lookup.The chop-chop growing size of routing tables brings with it the challenge to style main CAM design challenge is to scale back power consumption related to the massive quantity of parallel active electronic equipment, while not sacrificing speed or memory density.In this paper, CAM searchline design techniques at the circuit level for reducing power consumption are reviewed and presented.

Keywords: Content Addressable Memory, Throughput ,Searchline Power

Introduction

Content-addressable memory (CAM) compares input search value in parallel against a table of stored value, and returns the address of the matching value. Consequently, CAM cells contain storage reminiscences and comparison circuits. Because of its single clock cycle throughput, CAMs have a lot of quicker search systems than alternative hardware- and software-based; thus, CAMs are often utilized in a wide form of applications requiring high search speeds. the first industrial application of CAMs these days is to classify and forward internet protocol (IP) packets in network routers. In networks just like the web, messages like e-mails or sites are transferred by first breaking apart the messages into tiny information packets of some hundred bytes so causing every information packet on an individual basis via the network.From the source, these packets are routed via the intermediate nodes and reordered at the destination of the network to generate the first message. The operation of a router is to check the destination address of a packet to any or all doable routes so as to decide the suitable one. For instance, the present version of internet protocol (IP), usually referred to as IPv4, supports solely 32-bit Intenet Protocol addresses. Attributable to the fast increase within the range of net users, there's a growing scarcity of IPv4 addresses, that are required by all new devices connected to the web. Hence, a brand new version of IP (IPv6) has been introduced that supports 128-bit addresses.IPv6 is predicted to gradually replace IPv4. The increasing range of network nodes supported by IPv6 considerably will increase the capability and word-size of the routing table used for packet forwarding.

An economical hardware answer to perform table search operation is that the Content Addressable Memory. Because the vary of CAM applications grows, power consumption becomes one among the important challenges. The trade-off among power, speed, and area is that the most vital issue in recent researches on large-capacity CAMs. This paper can survey developments within the CAM area at circuit level primarily.

The remainder of this paper is organized as following.At first, in Section II we tend to illustrate the fundamental operation of CAM and also the core cells utilized in constructing the word block of CAM.Further, in Section III we tend to present varied searchline structures that are utilized in minimizing the searchline power and increasing the speed.

Operation of CAM

CAMs often contain a few hundred to 32 K entries for network routers, where each entry or word circuit contains several dozens of CAM cells. Each input-search bit is compared with its CAM-cell bit and the

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comparison result determines whether a pass transistor in the CAM cell attached to the match line (ML) of a word circuit is in on or off states.

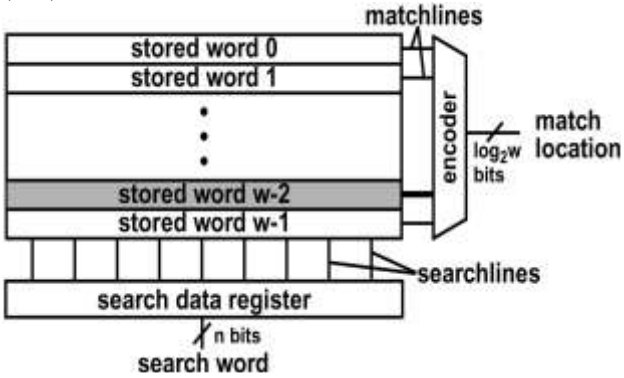

Figure. 1. Conceptual view of a content-addressable memory contains w words. In this example, the search word matches location (w-2) as indicated by the shaded box. The matchlines provide the row match results. The encoder outputs an encoded version of the match location using log_2w bits.

Figure.1 shows a simplified block diagram of a CAM.The search word is given as the input to the system is that is broadcasted onto the searchlines to the table of stored value. Each stored value has a matchline that shows whether the search data and stored data are same (the match case) or are different (the mismatch case).The matchlines are fed to an encoder which generates a binary match location according to the matchline that is in the match state. In CAM applications where more than one word may match, a priority encoder is utilized instead of a simple encoder.The highest priority matching location is given as input to the system to map to the match result, with words in lower address positions receiving higher priority. The overall operation of a CAM is to take a search word and return the matching memory position.

Core cell

A CAM cell can be classified into two types: NOR-type CAM cell [Fig. 2(a)] and NAND-type CAM cell [Fig. 2(b)].They serve two basic functions: bit storage (as in RAM) and bit comparison (unique to CAM).The bit storage uses an SRAM cell containing cross-coupled inverters. The bit comparison, which is logically equivalent to an XOR of the stored bit and the search bit is implemented in a somewhat different fashion in the NOR and the NAND cells[3].

A.NOR Cell

The NOR cell implements the comparison between the complementary stored bit, D and the complementary search value on the complementary searchline, SL, using four comparison transistors.M_1 through M_4, that are all usually minimum-size to keep up high cell density.The pulldown path of a dynamic XNOR gate with inputs SL and D is implemented by these transistors.Every combination of transistors, M_1/M_3 and M_2/M_4, forms a pulldown path from the matchline, ML, such a mismatch of SL and D allows least path of the pulldown paths, that connects ML to ground. A match of SL and D disables both pulldown paths, disconnecting ML from ground. The NOR nature of this cell becomes clear once multiple cells are connected in parallel to make a CAM word by shorting the ML of every cell to the ML of adjacent cells. The pulldown paths connect in parallel resembling the pulldown path of a CMOS NOR logic gate.Only if every individual cell in the word encompasses a match, there is a match condition on a given ML.

B.NAND Cell

The NAND cell implements the comparison between the stored value, D, and corresponding search value, on the corresponding searchlines ($SL, \overline{SL}$), using the three comparison transistors M_1,M_D and $M_{\overline{D}}$.Node B could be a pass-transistor implementation of the XNOR operate SL⊙D.The NAND nature of this cell becomes clear once multiple NAND cells are serially connected.During this case, the ML_n and ML_{n+1} nodes are joined to create a word. A serial nMOS chain of all the Mi transistors resembles the pull down path of a CMOS NAND logic gate.Only if every cell in a word is in the match condition a match condition for the entire word occurs.

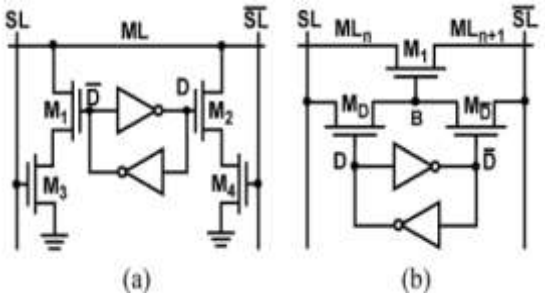

Figure. 2. CAM core cells for (a) 10-T NOR-type CAM and (b) 9-T NAND-type CAM [3].The cells are shown using SRAM-based data-storage cells.For simplicity, the figure omits the usual SRAM access transistors and associated bitlines.The SRAM storage and access transistors account for six of the cell transistors[3].

A NOR-type word circuit operates at high speed but it consumes large power dissipation. It is because mismatched word circuits discharge their ML capacitances to the ground line, where most of the word circuits tend to be mismatched in a CAM.In contrast, a NAND-type word circuit operates at

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medium speed.Because very few matched word circuits discharge their ML capacitances, a NAND-type word circuit reduces the power dissipation of MLs compared to the NOR-type word circuit.

CAM Search mechanisms

A.Conventional Approach

The conventional approach to driving the searchlines applies to matchline schemes that precharge the matchlines high.During this approach, during the search cycle, the searchlines are driven by a cascade of inverters first to their precharge level and then to their data value.The searchline power consumption depends on the searchline capacitance, which consists of wire capacitance and one transistor gate capacitance per row. The equation for the dynamic power consumption of the searchlines is

$$P_{SL} = 2n \times \frac{1}{2} C_{SL} V_{DD}^2 f \qquad (1)$$

$$= nC_{SL} V_{DD}^2 f \qquad (2)$$

where C_{SL} is the total capacitance of a single searchline, *n* is the total number of searchline pairs and V_{DD} is the power supply voltage. There are two searchlines per bit, which are precharged low and then charged to the appropriate search-data values. This results in two transitions per searchlines pair, or, equivalently, one transition per searchline.To this power, we must add the power consumption of the drivers. To maintain high speed, we drive the capacitance with drivers consisting of a cascade of inverters sized using exponentially increasing widths.When the searchline drivers are sized to minimize delay, the drivers add an overhead of about 25% to (1).

B. Eliminating Searchline Precharge

We can save searchline power by eliminating the SL precharge phase. Eliminating the SL precharge phase reduces the toggling of the searchlines, thus reducing power.The matchline-sensing schemes that precharge the matchline low eliminate the need for SL precharge, since activating the pulldown path in the NOR cell does not affect with matchline precharge.These schemes directly activate the searchlines with their search data without going through an SL precharge phase.Since, in the typical case, about 50% of the search data bits toggle from cycle to cycle, there is a 50% reduction in searchline power, compared to the precharge-high matchline-sensing schemes that have an SL precharge phase. The reduced power equation in this case is

$$P_{SL} = \frac{1}{2} \times nC_{SL} V_{DD}^2 f \qquad (3)$$

This equation shows that matchline-sensing schemes that precharge the matchlines low also save power on the searchlines.In fact, in these precharge-low schemes, the reduction in searchline power can be as large as, or even larger than, the reduction in matchline power.

C. Hierarchical Searchlines

Another method of saving searchline power is to shut off some searchlines by using the hierarchical searchline scheme.The basic idea of hierarchical searchlines is to exploit the fact that few matchlines survive the first segment of the pipelined matchlines. With the conventional searchline approach, even though only a small number of matchlines survive the first segment, all searchlines are still driven. Instead of this, the hierarchical searchline scheme divides the searchlines into a two-level hierarchy of global searchlines (GSLs) and local searchlines (LSLs).

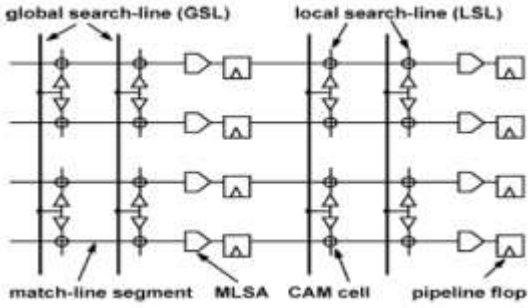

Figure. 3. Hierarchical searchline structure.

Figure.3 shows a simplified hierarchical searchline scheme, where the matchlines are pipelined into two segments, and the searchlines are divided into four LSLs per GSL.In the figure, each LSL feeds only a single matchline, but the number of matchlines per LSL can be 64 to 256. The GSLs are enabled each cycle, but the LSLs are enabled only when necessary. Enabling LSLs is essential when at least one of the matchlines connected by the LSL is enabled. In many cases, an LSL will have no enabled matchlines in a given cycle; hence there is no need to activate the LSL, saving power. Thus, the overall power consumption on the searchlines is

$$P_{SL} = \left(\underbrace{C_{GSL} V_{DD}^2}_{GSL} + \underbrace{\alpha n C_{LSL} V_{DD}^2}_{LSL} \right) f \qquad (4)$$

D. Self-Timed Charge Recycling Searchline

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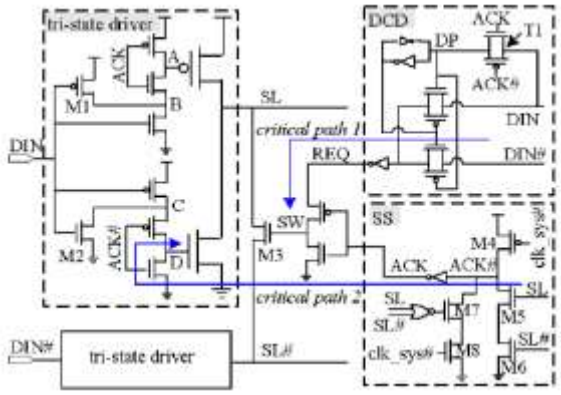

Figure. 4.Self-timed charge-recycling SL driver. Here, DCD denotes data change detector, and SS denotes state sensor[3].

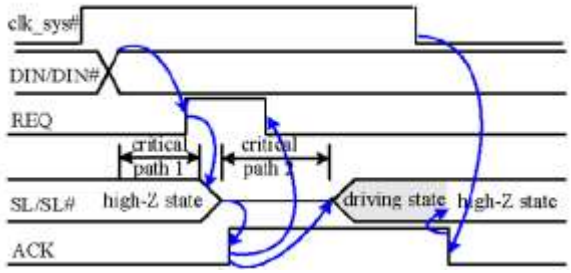

Figure. 5.Timing for the proposed self-timed charge-recycling driver[3].

Figure.4 shows the proposed self-timed charge-recycling driver circuit[3].As can be seen, the self-timed driver (STD) is mainly composed of three parts: data change detector (DCD), state sensor (SS), and tri-state driver. Assume the CAM system pre-charges/evaluates during the low/high level of the system clock clk_sys.The self-timed driver analyzes during low clk_sys to provide search key to CAM. During high clk_sys, SL/SL# is floating and the control logic of STD stays in pre-charge state. The whole STD works in a request-and-acknowledge style with the timing chart shown in Figure.5.When DCD detects that new search key (DIN, DIN#) comes during low clk_sys (clk_sys# = 1), a request signal REQ is asserted (REQ = 1).Then charge sharing occurs between SL and SL# via transistor M3. After the end of charge sharing, that is SL and SL# has equal voltage, or V(SL) = V(SL#), SS asserts an acknowledge signal ACK (ACK = 1). Finally, SL and SL# update their value and REQ is de-asserted. Also ACK is deasserted by high clk_sys.

There are two critical paths in Fig.5: Critical path 1 is from the coming of new search key to the switching on of M3, and Critical path 2 is from the detection of the end of charge sharing to the beginning of STD updating its value. Each path introduces 3 gates delay while the conventional charge recycling driver totally spends delay of 8 gates.

Instead of needing an additional clock which has stringent requirements both in phase and pulse width with the system clock as in the conventional charge sharing driver, the proposed scheme can self-sense the completion of the charge sharing process between SL and SL#. The delay overhead of the control logic was reduced from delay of 8 to 6 gates.

E.Synchronous Word Overlapped Searchline

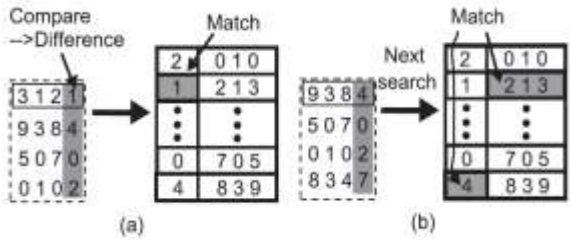

Figure. 6. Synchronous Word-Overlapped Search (SWOS) (m=3). As long as the last k bits of the current search word are different from those of the subsequent m search words, the next search is initiated after the current k-bit sub-search is complete[2].

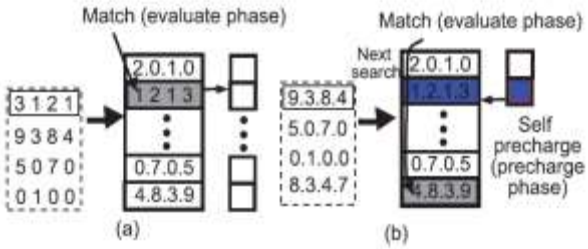

Figure. 7. Self precharging in Synchronous Phase-Overlapped Processing (SPOP). A match operation (evaluate) is initiated during precharging a match line of another word block (precharge) that operates as a match at the previous clock cycle[2].

The synchronous overlapped search mechanism (SOSM)[2] is a high-speed data search mechanism that enables a next-word search after searching just a few bits of the current word by simple pre-computation.A SOSM includes two approaches: a Synchronous Word-Overlapped Search (SWOS)[2] and Synchronous Phase-Overlapped Processing (SPOP)[2].Figure.5 shows the SWOS scheme in CAM that operates in one of the two modes: fast and slow.Before searching words in CAM, the last *k* bits of the current search word are compared with the *k*-bit subsequent *m* sub words in the input controller shown in Figure. 6(a). If they are different, the next search is initiated as soon as the current *k*-bit sub-

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word search is complete shown in Figure. 6(b).As long as the last *k* bits of the current search word is different from those of the subsequent *m* search words in the input controller, search words are assigned to unused different word blocks and hence are processed at a rate based on T_{1st}.This is the fast mode.

When the consecutive sub-search words are found to be the same, the next sub-search word is assigned to the same sub-word blocks in which the current sub-search word matches. The matched sub-word blocks are initialized after the current search has completed in both segments.As the search time of the second segment is denoted by mT_{1st}, the next search is initiated $(1 + m)T_{1st}$ after the current search is initiated. This is the slow mode.The average search time based on the proposed SWOS scheme T_{avg} is given by

$$T_{avg} = T_{1st}\left(1-\left(\frac{1}{2}\right)^k\right)^m + (1+m)T_{1st}\left(1-\left(1-\left(\frac{1}{2}\right)^k\right)^m\right) \quad (5)$$

In the proposed SPOP scheme, each word circuit is designed based on the NAND-type structure and is independently controlled using a self-precharge block shown in Figure.7(a).In the word circuits, match line (ML) capacitances of only matched word circuits are discharged while ML capacitances of mismatched word circuits remain. The ML capacitances of the matched word circuits are then precharged by their self-precharge blocks in the precharge phase in Figure.7(b).In contrast, other word circuits that were previously mismatched still operate in the evaluate phase to keep the match operation of the CAM for the next search word.

F.Reordered Word-Overlapped Searchline

The Reordered Word-Overlapped Search scheme (RWOS) reduces the probability of the slow mode to improve the throughput. In this scheme, the last *k* bits of a current search word are compared with the *k* last bits of consecutive search words and an extra search word followed by the current search word. If the *m* consecutive sub-search words are different from the current sub-search word, the CAM operates at the fast mode. Otherwise, one of the *m* sub-search words that is the same as the current sub-search word is replaced by the extra sub-search word. In this case, the extra sub-search word has to be different from the current sub-search word. In the example shown in Figure.8(c), the current sub-search word is "A", while the input buffer has "B", "A", and "C".In this case, as the second sub-search word "A" is replaced by the extra sub-search word "D," the current sub-search word "A" is different from all *m* consecutive sub-search words in the input buffer. Therefore,the CAM keeps operating at the fast mode. The average search time based on the proposed RWOS scheme T_{SAR} is given by

$$T_{SAR} = T_{fast}p_{fast} + T_{slow}(1-p_{fast}) \quad (6)$$

$$p_{fast} = \left(1+m(p_s)^k\right)\left(1-(p_s)^k\right)^m \quad (7)$$

The cycle time in the reordered overlapped search mechanism based on the RWOS and POP schemes is given by

$$T_{CAR} = T_{SAR} \quad (8)$$

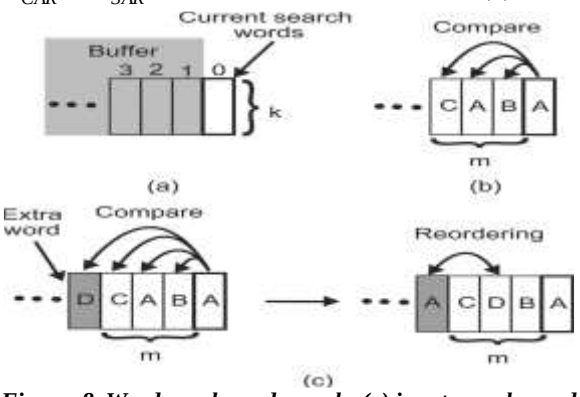

Figure. 8. Word-overlapped search: (a) input search-word buffer, (b) the word overlapped search mechanism, and (c) the proposed reordered word-overlapped search mechanism. If the last k bits of a search word is the same as at least one of m sub-search words, the search word is replaced by an extra search word to keep the CAM operate at fast mode.

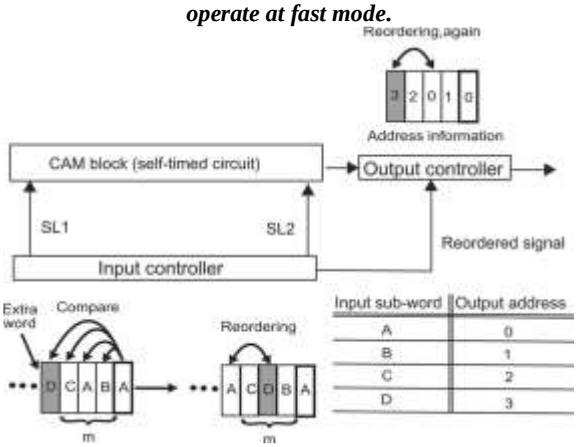

Figure. 9. High-level structure of the proposed CAM based on the RWOS and the POP schemes. Once input words are reordered, the output addresses correspond to the input words are reordered, again by indicating which address is replaced.

Figure.9 shows the high-level structure of the CAM based on the RWOS and the POP schemes.It contains a CAM block, an input controller, and an output

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controller. Each last *k*-bit input sub-word is corresponding to its output address shown in the table of this figure.Once input words are reordered in the input controller, the input controller sends a signal, which indicates a reordered input word to the output controller. The output controller reorders the output address based on the signal.

Conclusion

In this report, we have surveyed CAM circuits, with an emphasis on high-capacity and high-speed CAM. First, we motivated our discussion by showing basic operation of CAM with respect to packet forwarding in network routers. We have reviewed the two basic CMOS cells, namely the NOR cell and the NAND cell.Finally, we have reviewed the conventional approach for driving searchlines, the power-saving approaches which eliminate the searchline precharge or employ hierarchical searchlines or half-timed charge recycling, and the high-speed approaches, synchronous word overlapped searchline and reordered word overlapped searchline which eliminate the delay overhead by improving the throughput.

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